Synopsis for Registration as Research Student
For
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On
Design and Implementation of Some Digital Signal Processing Blocks

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1. Introduction

Digital signal processing (DSP) is the process of analysing the signal in digital form and extracts the useful information carried out by signal. Nowadays, DSP is the heart of modern world. DSP powers the modern communication (voice recognition), modern entertainment (motion-sensing game) and tomorrow's inspiration is to make autonomous vehicle. DSP is also used in applications like Biometric Security Systems, Brain-Computer interface to study emotions, Hearing aids, Speech Synthesis, Digital Cameras for affordable photography, Ultrasonic Machines for better and safer medical scan, 3D television, Weather Forecasting, Seismology etc.

There are basically three operations: delay, addition and multiplication. With this, one of the most widely used signal processing operation is filtering whose main objective is to alter the spectrum according to some given specification. Filter is used to extract the useful portion of interest and remove the unwanted portion such as noise, which is generated due to unavoidable circumstances of the environment, from the input signal. Digital filters, due to number of advantages such as high accuracy and reliability, small physical size, and reduced sensitivity to component tolerances are better choice over analog filters. Also, the digital filters are programmable, which means that the characteristics of digital filters can be easily modified leaving the hardware unchanged.

In general, digital filters can be classified into two categories according to the duration of their impulse responses, finite-duration impulse response (FIR) and infinite duration impulse response (IIR). An FIR digital filter is known as a non-recursive digital filter as it does not have the feedback and an IIR digital filter is referred as a recursive digital filter as tit has feedback. An FIR filter is absolutely stable filter and gives exact linear phase while IIR filter gives non-linear phase and may be stable or unstable. Both FIR and IIR filters are designed using various methods given in literature. FIR filter is designed using approximation techniques and IIR filter derived from analog design. Both filters are realized and implemented using various types of filter structures available like direct form structure, cascade structure or lattice structure. Efficiency of filter is decided by filter order and measured in terms of number of multipliers, adders and delay elements required for realizing the filter. For any given set of required filter characteristics, FIR implementation will require higher order filter and more memory than an Infinite Impulse Response (IIR) implementation.

A multi-rate filter is a digital filter that changes the input sampling rate of the input signal into another desired one. Basic building blocks of multi-rate systems are up-sampler to increase sampling rate and down-sampler for reducing sampling rate. Filtering is required to suppress aliasing when reducing the sampling rate, called as decimation, and to remove unwanted imaging when increasing the sampling rate, called as interpolation. The use of an appropriate filter enables one to convert a digital signal of a specified sampling rate into another signal with the desired sampling rate without significantly destroying the signal components of interest. In many cases, instead of using a single-stage system, it is more beneficial to carry out the overall procedure with a multistage system as it reduces the arithmetic complexity. Also, it is necessary that the filtering is performed at the lowest sampling rate which results in a low computational complexity (i.e., few multiplications and additions per sample are required)

The efficiency of FIR filters for sampling rate conversion is significantly improved using the polyphase realization. Filtering is embedded in the decimation/interpolation process and a poly-phase structure is used to simultaneously achieve the interpolation/decimation by a given factor but running at a low data rate. Due to the polyphase multi-rate implementation, the number of arithmetic operations in a linear phase FIR filter is decreased by a factor decimation (M)/interpolation (L).

The field of DSP has always been driven by the advances in DSP applications and in scaled very-large-scale-integration (VLSI) technologies. Therefore at any given time, DSP applications impose several challenges on implementation of the DSP systems. This implementation must satisfy the sampling rate constraints of the real time DSP applications and must require less space and power consumption. The DSP computation is different from general-purpose computation in the sense that DSP programs are non-terminating programs. In DSP computations, the same program is executed repetitively on an infinite time series. The non-terminating nature of DSP program/algorithm limits the performance of DSP systems. These algorithms need to be transformed for the design of high speed or low area or low power implementations. The several high-level architectural transformations can be used to design families of architecture for a given algorithm. The transformation includes pipelining, retiming, unfolding, folding and systolic array design methodologies. The high level algorithm transformation such as strength reduction, look-ahead and relaxed look-ahead. Strength reduction transformation is applied to reduce the number of multiplications in convolution, parallel FIR digital filters, discrete cosine transforms (DCTs) and parallel rank-order filters. Look-ahead and relaxed look-ahead transformations are applied to design pipelined direct-form and lattice recursive digital filters and adaptive digital filters and parallel recursive digital filters.

2. Literature Survey

The challenge of efficient digital filter design is one of the fundamental goals of digital signal processing. Various methods for digital filter design are given in [1]-[4].

Y. Neuvo et al. [5] proposed a new approach to implement computationally efficient finite impulse response (FIR) digital filters based on interpolation of the impulse response is called as Interpolated FIR (IFIR) filter. This method is used to implement narrowband lowpass FIR filter designs with a significantly reduced computational complexity relative to traditional FIR filters.

T. Saramaki et al. [6] presented two methods for designing efficient FIR filters with same input and output rates. In first method, the shaping filter and the interpolator of the IFIR filter structure were simultaneously optimized with a method based on the Remez multiple exchange algorithms. And in second method, an efficient interpolator was derived using recursive running sum interpolator which further reduced the number of arithmetic operation required in IFIR implementation.

A. Mehrnia and A. J. Willson [7] investigated an analytical approach for determining the optimum stretch factor in IFIR designs. This is important because the choice of stretch factor affects the efficiency of the method. This approach also illustrates the sensitivity of the complexity versus the variation of the stretch factor for a given design specification.

G. J. Dolecek and S. K. Mitra [8] proposed a new computationally efficient structure for a sharpened comb-rotated sinc (RS) decimator. The decimator is composed of two main sections. The first section is a cascaded comb decimator, while the second section is a cascade of a sharpened comb and a rotated sinc (RS) decimator. The proposed decimation filter has much smaller pass-band droop and much better alias rejection than the original RS filter.

G. J. Dolecek and S. K. Mitra [9] presented two-stage multiplierless cascaded-integrator-comb (CIC) based decimator. The first stage is a cascaded CIC filter whereas the second stage is a cascaded CIC filter and a second-order multiplierless compensator. The proposed decimator can be realised without filtering at high input rate by making use of the polyphase decomposition of the comb filter in the first stage. The proposed filter exhibits high aliasing attenuation and a low passband droop.

M. Laddomada et al. [10] proposed the design of multiplierless decimation filters using an extended set of cyclotomic polynomials (CPs) as constituent's filters. All the CPs with indexes extended to the set {1,. . . ,200} have a z-transfer function whose coefficients are simply {-1,0,+1}. This property makes these polynomials very well suited to computationally efficient filter architectures.

D. Shi and Y. J. Yu [11] suggested a general-purpose algorithm for the design of linear phase FIR filters in cascade form with discrete coefficients. The proposed algorithm decomposes the overall filter into sub-filters during the traverse of MILP search of the overall filter. The proposed algorithm achieves significant reduction in both implementation cost and adder depth compared with their single-stage optimum designs.

E. R. Pelet [12] used interpolation filter for proper recovery of the transmitted data in quadrature amplitude modulation(QAM) signal often requires a digital resampling in the receiver to produce samples at the correct decision times. This paper gives a n closed form equation which relates the mean-squared error (MSE) to the frequency response of the interpolation filter so that error free new sample can generate. This equation includes the effect of additive Gaussian noise and timing jitter.

Z. Sheikh and O. Gustafsson [13] proposed a linear programming formulation for reconfigurable FIR filters based on the coefficient decimation technique. The technique is based on decimating and/or interpolating a fixed set of impulse response coefficients. In this way, several different frequency responses are obtained without changing the coefficient values. Hence, there is no need to store different filter coefficient sets and techniques for simplifying the multipliers, such as shift-and add techniques, can be straightforwardly applied.

Y. Wei and D. Liu [14] proposed a novel 2–stage Frequency Response Masking (FRM) structure for sharp FIR filter. The three interpolation factors of the sub-filters in the second stage can be chosen independently. The band-edge shaping filter synthesized by the second stage has a non-periodical frequency response, which is quite different from conventional FRM structures. The proposed method has significant savings in terms of the number of multiplications as compare to current FRM schemes. Both the complexity and the group delays are reduced.

H. Johansson and A. Eghbali [15] proposed add-equalize structures for implementation of linear phase nyquist FIR filter interpolators and decimators. . In the proposed structures, the polyphase components share common parts which lead to a considerably lower implementation complexity as compared to conventional single-stage converter structures. Main advantage is that they work equally well for all integer conversion factors, thus including prime numbers which cannot be handled by the regular multi-stage Nyquist converters.

H. Johansson and H. Gockler [16] proposed efficient two stage based polyphase structures for arbitrary integer sampling rate conversion. For the linear-phase finite-length impulse response M^{th} band filters, it is then demonstrated through design examples that conversions by odd factors are in fact more efficient than by even factors.

A. Mehrnia and A. N. Willson [17] presented a further-desensitized halfband filter design and corresponding direct-form and transposed-type structures for its implementation. The new filters are constructed as a cascade of a sub-filter and $(1 + z^{-1})^2$ block. For halfband filters designed this way, the sensitivityof the filter to its coefficients can be systematically reduced in comparison with conventional designs.

A. Mehrnia and A. N. Willson [18] suggested that the most efficient FIR digital filters can be created by using a scaled sequence of stages, each representing a factor of filters transfer function. The efficiency of the resulting structure depends heavily upon obtaining such optimal factors. This paper gives an algorithm to find, scale and sequence optimally factored FIR filters.

A. Mehrnia et al. [19] used halfband filters in radio frequency/intermediate frequency data converter to interpolate or decimate the signal responsible for a considerable portion of the power consumption. The sensitivity of halfband filters to coefficient quantization can be systematically reduced. This can be used in filter design process to yield reduced hardware complexity and leading to power consumption and higher operating speeds.

D. Lamb et al. [20] suggested a novel efficient structure for spline interpolation/decimation using fractional delay filtering. First, the Newton structure was derived using a series of transformations of the Farrow-Lagrange structure. These transformations were applied to the spline coefficient matrix yielding a novel Newton-like structure for spline interpolation.

D. Shiung et al. [21] suggested a novel method for designing high performance FIR filter with less complexity. This method is for improving the frequency response of an FIR filter by cascading it with complementary comb filter (CCF). Thus, the composite filter (cascading of low order FIR filter and CCF's) approaches an ideal lowpass filter more closely in both the transition band and stopband. Because a CCF contains only one adder and a few storage units, the cost is minimal.

A. Ambede and A. Vinod [22] proposed the generalized design procedures and modified pipelined hardware implementation architectures for the first- and second-order all-pass transformation (APT)-based variable digital filters (VDF). Multiple first- and second order APT-based VDFs were designed, and their FPGA implementation results obtained using the conventional non-pipelined and the proposed pipelined implementation architectures were presented. An analysis of the results showed that the proposed pipelined implementation

architectures enabled high operating frequencies that were independent of the different prototype filter orders, for both the first and second-order APT-based VDF designs.

I. Hatai et al. [23] proposed a two-step optimization technique for designing a reconfigurable VLSI architecture of an interpolation filter for multi-standard digital up converter (DUC) to reduce the power and area consumption. The proposed technique initially reduces the number of multiplications per input sample and additions per input sample by designing a root-raised-cosine finite-impulse response filter for multi-standard DUC for three different standards. In the next step, a 2-bit binary common sub-expression (BCS)-based BCS elimination algorithm has been proposed to design an efficient constant multiplier, which is the basic element of any filter.

S. J. Darak et al. [24] presented a computationally efficient variable digital filter (VDF) using warped filter and coefficient decimation (CDM) technique. The proposed architecture provides variable lowpass or highpass responses with fine control over cut-off frequency and variable bandwidth bandpass or bandstop responses at an arbitrary centre frequency without updating the filter coefficients or filter structure.

Y. Tsao and K. Choi [25] proposed new 3-parallel FIR digital filter structures for symmetric convolution of odd length, which save significant amounts of multipliers at the expense of increase of additional adders. The proposed 3-parallel FIR structures exploit the inherent nature of symmetric coefficients of odd length with the proposed polyphase decompositions. Hence this structure can lead to significant hardware savings especially when the length of the filter is large.

J. Li et al. [26] presented a high-speed low-power decimation filter design in VLSI implementation. The decimation filter consists of a comb-filter and two half-band filters (HBF). Its power consumption is reduced by adopting poly-phase decomposition technique, multiplierless filter architecture and hardware re-usage. This filter is a part of a broadband and high resolution sigma-delta A/D converter.

3. Problems Identified

- To design computationally efficient narrowband FIR/IIR digital filter using multi-rate techniques.
- To investigate new efficient digital filter structures
- To investigate polyphase decomposition for different filter structures.
- To design FIR/IIR Single tone/Multi-tone filters using multi-rate technique.
- Reducing hardware complexity (i.e. reducing storage in the system) and making it cost efficient implementation of digital filter using multi-rate techniques.
- VLSI Implementation of FIR/IIR digital filter using multi-rate technique.

4. Conclusions

It is possible to design and implement efficient digital filter using multi-rate techniques. The method suggested as probable solution like interpolated filter design method with combination of polyphase representation can give us better solution for identified problems. Further digital filter can be implemented in VLSI so that design should be power and area efficient.

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